

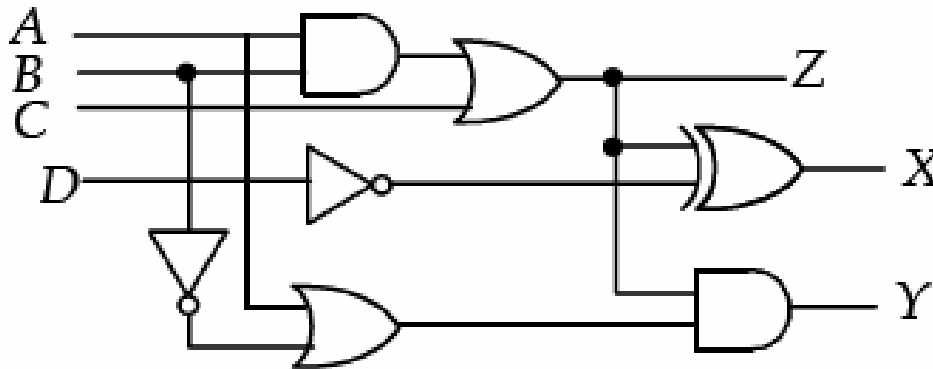


Lab Assignments for VHDL and its Practice (I)

Lecturer: Prof. S. Chang

**Dept of Electrical and Computer Engineering
University of Seoul**

Assignment 1



1. Write a dataflow VHDL description for the above circuit diagram. Include the VHDL code in your **pre-lab report**.
2. Compile and synthesize the VHDL code using Xilinx tool. You will obtain a schematic diagram and design information from schematic view and map report, respectively. Include the results in your **post-lab report**.
3. Make your test-bench for full simulation of the VHDL code. Simulate it using ModelSim. You will obtain a wave result. Include it in your **post-lab report**.
4. Compare your wave result with the expected one, and discuss in your **post-lab report**.



Assignment 2

1. Write a dataflow VHDL description for an 8-to-1-line multiplexer based on the VHDL code in pp. 9 of the lecture note. Include the VHDL code in your **pre-lab report**.
2. Compile and synthesize the VHDL code using Xilinx tool. You will obtain a schematic diagram and design information from schematic view and map report, respectively. Include the results in your **post-lab report**.
3. Make your test-bench for full simulation of the VHDL code. Simulate it using ModelSim. You will obtain a wave result. Include it in your **post-lab report**.
4. Compare your wave result with the expected one, and discuss in your **post-lab report**.



Assignment 3

Truth Table of Priority Encoder

Inputs				Outputs		
D ₃	D ₂	D ₁	D ₀	A ₁	A ₀	V
0	0	0	0	X	X	0
0	0	0	1	0	0	1
0	0	1	X	0	1	1
0	1	X	X	1	0	1
1	X	X	X	1	1	1

- Design an optimized logic diagram for the truth table. Include it in your **pre-lab report**.
- Write a dataflow VHDL description for the logic diagram based on the VHDL code in pp. 9 of the lecture note. Include the VHDL code in your **pre-lab report**.
- Repeat the procedure 2, 3, and 4 in the assignment 1.