



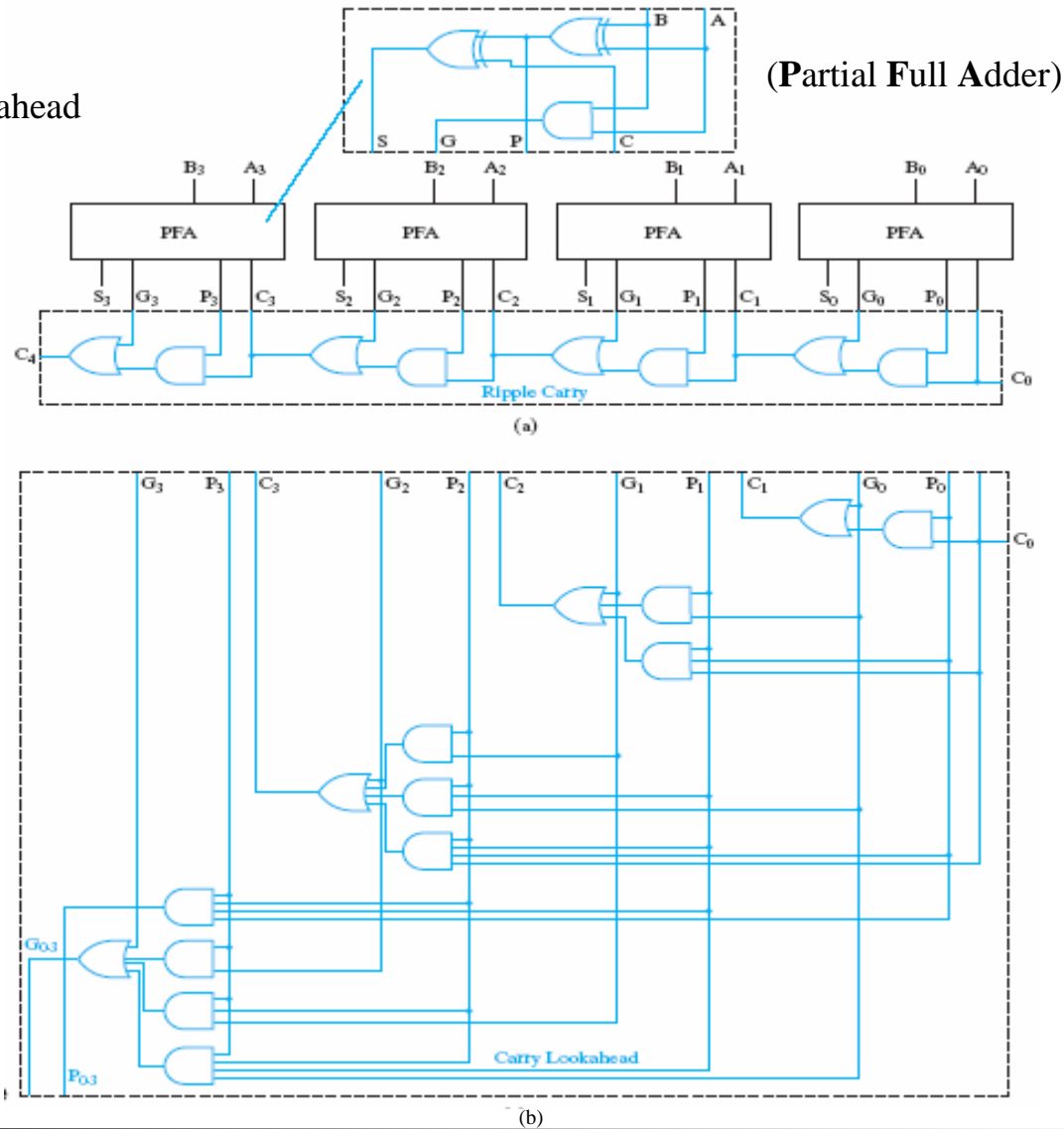
Lab Assignments for VHDL and its Practice (II)

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Assignment 2

Fig. 1 4-Bit Carry Lookahead Adder





Assignment 2 (continued)

- Write a hierarchical VHDL description based on the VHDL code in pp. 4 and pp. 5 of the lecture note for the circuit diagram of Fig1. Include the VHDL code in your **pre-lab report**.
- Repeat the procedure 2, 3, and 4 in the assignment 1.



Assignment 3

Characteristic table of JK flip flop

J	K	$Q(t+1)$
0	0	$Q(t)$
0	1	0
1	0	1
1	1	$Q'(t)$

- Write a VHDL description for a negative-edge-triggered JK flip-flop without reset (Use *process* module). Include the VHDL code in your **pre-lab report**.
- Repeat the procedure 2, 3, and 4 in the assignment 1.